0.5-2.6GHZ Si-MONOLITHIC WIDEBAND AMPLIFIER IC

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ABSTRACT

Using Si, an excellent performances, 0.5-2.6GHz bandwidth and 23dB gain, monolithic wideband amplifier IC has been developed, of which input and output impedances are matched to 50Ω. The f_T=10GHz DNP-II manufacturing process with optimization for microwave analog ICs has been developed for this IC. And a single-ended three stages amplifier circuit with local feedback loops is adopted for this monolithic circuit.

INTRODUCTION

DBS(Direct Broadcasting Satellite System) had been started, and its receiver will become popular. However, cost reduction is indispensable doing this. We tried, with cheaper Si material, to develop a monolithic IC of 0.9-1.8GHz 1st-IF stage amplifier which was constructed by discrete devices with complicated tuning, up to the present.

We have already reported f_T=6.3GHz DNP-I(Direct Nitride Passivated base surface-I) manufacturing process that was applied to a 1.4GHz wideband amplifier IC [1], and enhanced f_T=10GHz DNP-II process that was applied to a microwave prescaler IC [2]. In this study, in order to achieve a 2GHz wideband amplifier IC, we developed the improved DNP-II process with optimization for microwave analog ICs.

The monolithic circuit described here is a single-ended three stages amplifier circuit with local feedback loops, which achieves a high gain, a low noise figure and an impedance matching to 50Ω lines.

In this paper, the processing technique, circuit design and performances are described.

PROCESSING TECHNIQUE

In order to realize an analog IC function in the microwave frequency range, the manufacturing process conditions are determined and the transistor cells are designed according to the following policies based on the DNP-II process.

1. Achieving f_T=10GHz, a base resistance is reduced in order to prevent degradation of both insertion gain $|S_{21}|^2$ and noise figure.
2. For a low distortion performance, a gain reduction doesn't occur until collector current IC=20mA.
3. To realize the circuit biasing V_{CC}=12V, a collector-emitter breakdown voltage is designed BV_{ceo}>10V.

Fig. 1 shows a cross sectional view of improved DNP-II transistor cell which possesses the following features;

1. To achieve f_T=10GHz and lower base resistance, a shallow(Xjc=0.2um) and higher impurity doped (Nb=1x10^{18} atom cm^{-3}) base is formed by ion implantation and lamp annealing. A shallow emitter(Xj_E=0.1um) is formed by drive-in from As-doped polysilicon.
2. To reduce the base resistance and the E-B junction capacitance, an emitter of 1um width is formed.
3. To achieve BV_{ceo} > 10V, epitaxial layer thickness and resistivity are optimized.
4. To form high reliable electrodes, a Ti-Pt-Au electrode structure is adopted.

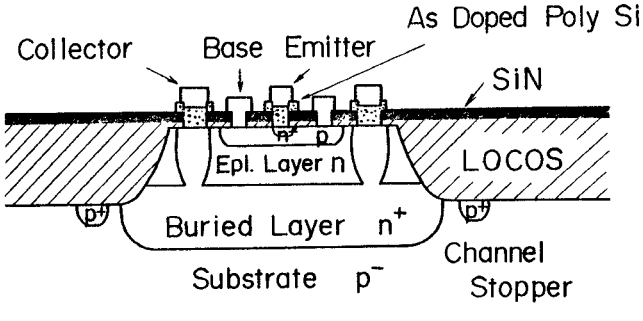

Fig. 1 A cross sectional view of transistor cell.

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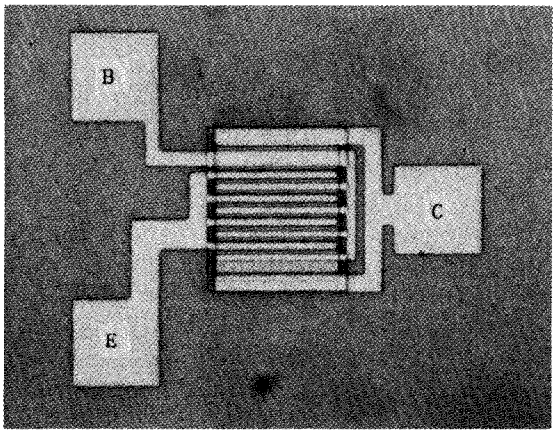

Fig. 2 Microphotograph of transistor cell.

Table 1. Transistor cell dimensions and device parameters.

Emitter width		1 μm
Emitter length		40 X 4 μm
Base area		1596 μm^2
Collector area		2880 μm^2
Minimum electrode width		2 μm
Minimum electrode space		2 μm
BVcbo		25V
BVceo		12V
hFE		100
fT		10GHz
Satulation current	Is	2 x 10^{-16}A
Base resistance	rb	12Ω
Emitter resistance	re	0.3Ω
Collector resistance	rc	9.4Ω

Resistances are formed by p^+ doped polysilicon on the thick field oxide layer to reduce parasitic capacitance. The transistor cell photograph is shown in Fig. 2 and its gain vs. collector current characteristics are shown in Fig. 3. Fig. 3 means that f_T=10GHz is achieved at IC=20mA. Also, the optimum noise figure of this transistor is 2dB at f=2GHz.

Table I shows the dimensions and device parameters of the transistor cell shown in Fig. 2.

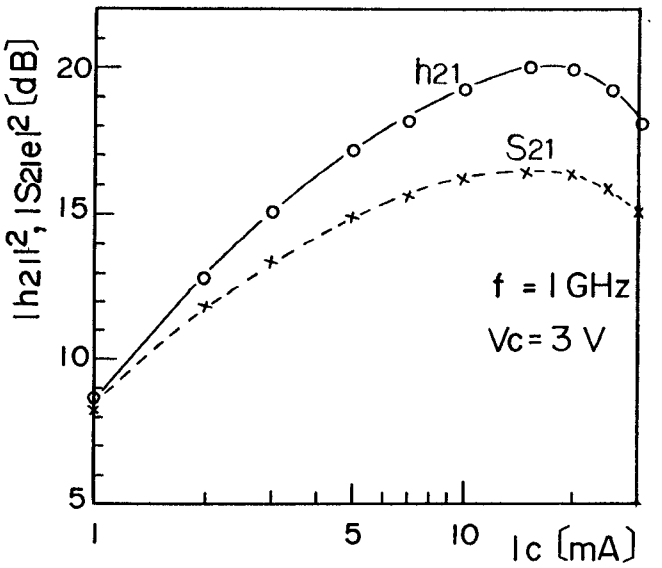

Fig. 3 Gain vs. collector current of transistor cell.

CIRCUIT DESIGN

Either differential type or single-ended type circuit is available for construction of a wideband monolithic amplifier. In this paper, a single-ended three stages circuit with local feedback loops has been adopted for the following reasons;

1) Higher gain is obtained with less bias current.
2) Owing to the smallness of the input-stage emitter resistor, the noise performance is superior to that of the differential type circuit.
3) The input and output impedances are easily adjusted.
4) A good isolation characteristic is available due to the three stages amplifier.

The optimized circuit is shown in Fig. 4. A local feedback loop is adopted in each stage for stability at higher frequency. The coupling capacitor between 2nd and 3rd-stage is used for compensation of gain flatness and simplifying DC bias design. In each stage, emitter peaking are adopted with peaking capacitor C_{E1}, C_{E2} and C_{E3}.

Circuit parameter optimization is done with the use of the circuit analysis program SPICE-2.

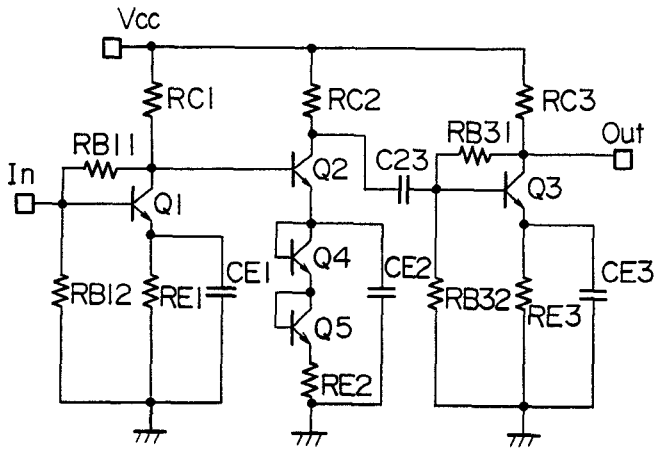

Fig. 4 A three stages amplifier circuit.

CHIP LAYOUT DESIGN AND RESULTS

A die photograph is shown in Fig. 5. Areas of bonding-pad are designed $100x100um^2$ for ease of bonding. Three ground bonding-pads are provided in order to reduce the effect of bonding wire inductance.

The frequency dependences of S-parameters measured with a strip-line type package are shown in Fig. 6. The gain $|S_{21}|^2$ is 23dB at flat zone and -3dB bandwidth is 0.5~2.6GHz. Because of $|S_{21}|^2 \approx 10$dB at 4GHz, it is possible to make a 4GHz wideband amplifier by changing the circuit parameters. The input and output return losses, $|S_{11}|^2$, $|S_{22}|^2$ are below -8dB, and the excellent isolation characteristic $|S_{12}|^2 < -40$dB is achieved. Therefore in the practical application, it is easy to construct a 46dB gain wideband amplifier with cascade connection of two present ICs. Fig. 7 shows the frequency dependence of noise figure. 4.8dB noise figure is achieved at f=1.5GHz. Fig. 8 shows the output power vs. input power characteristic at f=1.5GHz. The saturation power of 2.5dBm is obtained in Fig. 8.

RF performances are listed in Table2.

CONCLUSIONS

A Si-monolithic wideband amplifier with 0.5-2.6GHz bandwidth, 23dB gain and 4.8dB noise figure has been developed. With the present ICs, it is able to manufacture more compact and cheaper DBS receivers.

The present amplifier IC have 10dB gain at 4GHz, so it is indicated that a 4GHz wideband amplifier can be realized with Si material now.

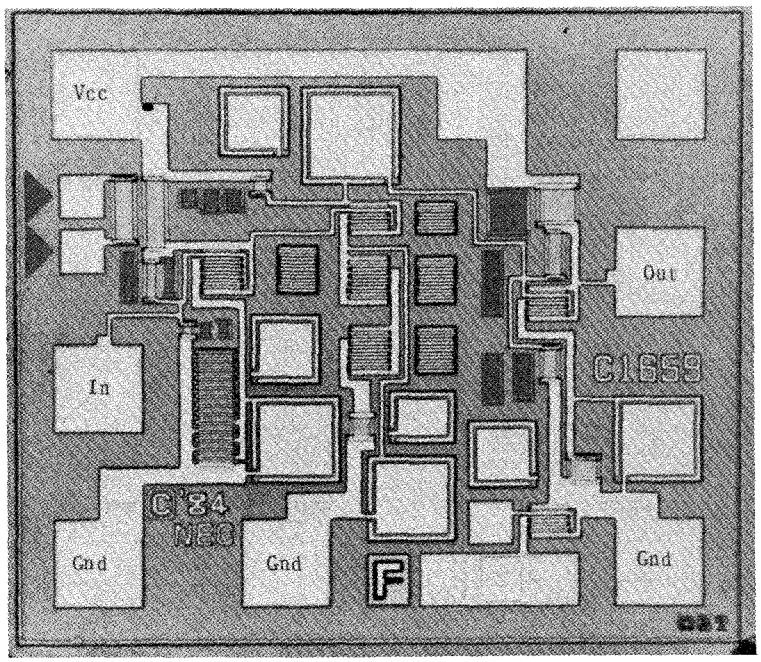

Fig. 5 Microphotograph of amplifier die.

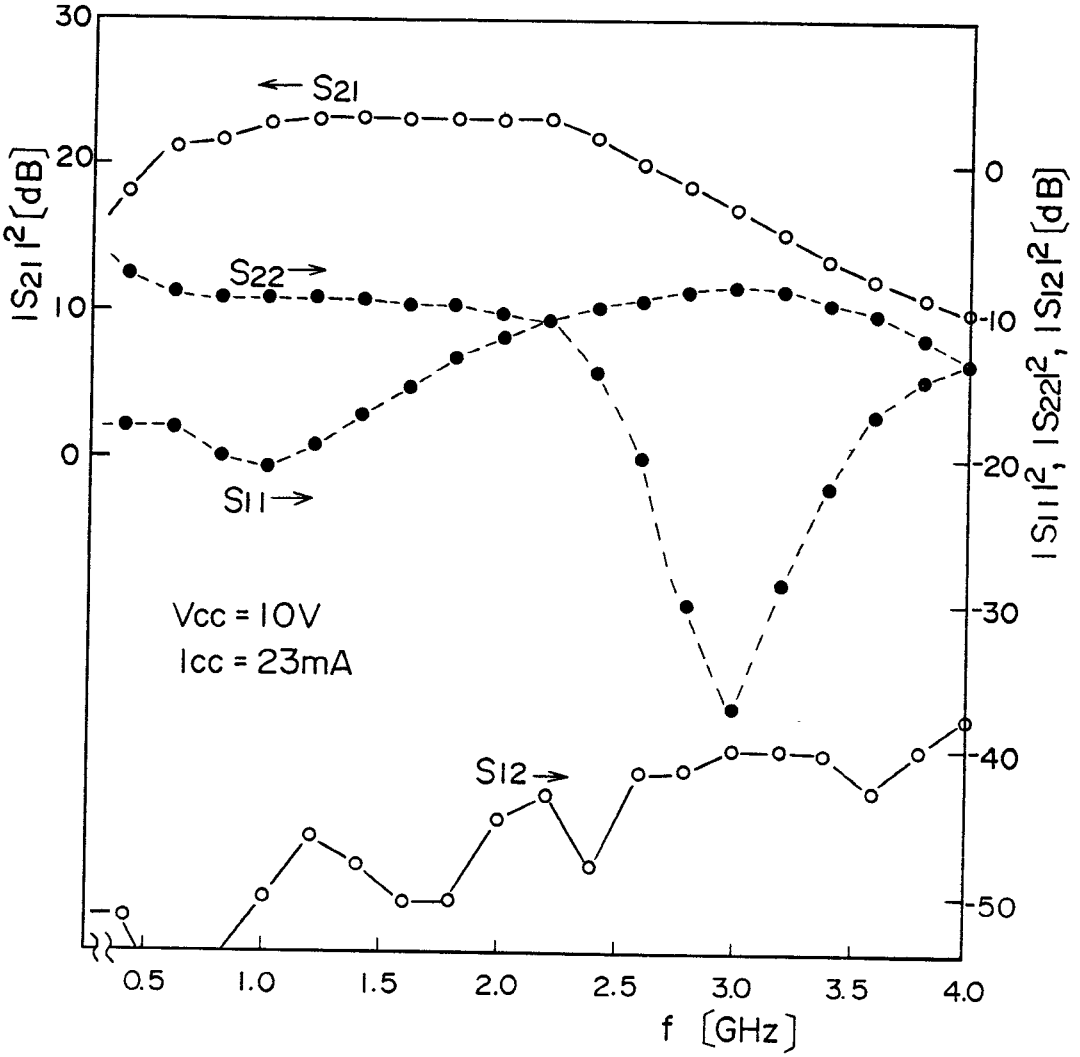

Fig. 6 Frequency dependences of S-parameters.

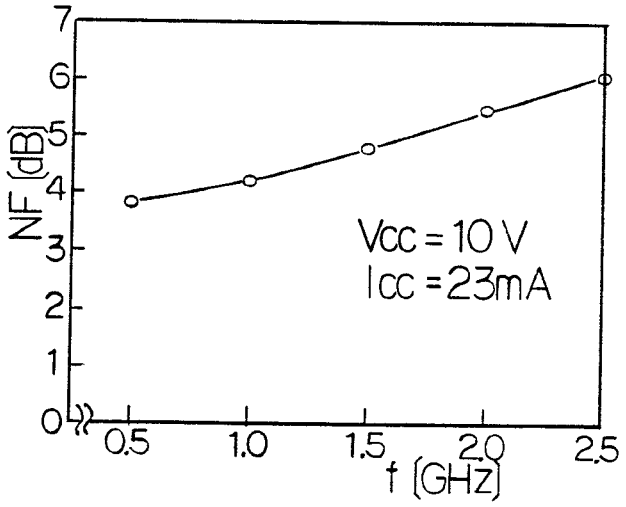

Fig. 7 The frequency dependence of noise figure.

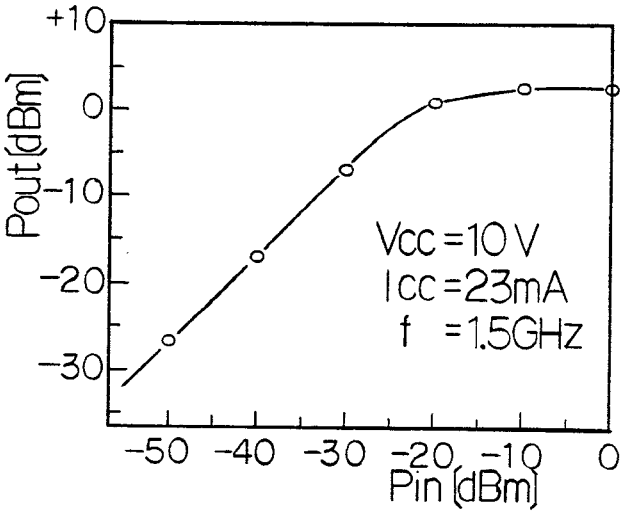

Fig. 8 Output power vs. input power

Table 2. RF performances

Bandwidth	(3dB down)	0.5 ~ 2.6GHz
Gain	$\|S_{21}\|^2$	23dB
Return loss	$\|S_{11}\|^2$	<-8dB
Return loss	$\|S_{22}\|^2$	<-8dB
Reverse gain	$\|S_{12}\|^2$	<-40dB
Noise figure	(f=1.5GHz)	4.8dB
Psat.	(f=1.5GHz)	2.5dBm
IM_3	(Po=-10dBm, f=1.5GHz)	- 45dB

ACKNOWLEDGMENTS

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